**Objective:**

The objective of the project is to understand the basic operation of arithmetic logic unit of computer processor and for this we design 16 function which can perform 16 different task. Among them 12 are functions can perform arithmetic operation and 4 functions can perform logical operation.

**Task and Function distributions:**

We have to design 4 bit ALU(Arithmetic Logic Unit). For this, we input two 4 bit number and one 4 bit selection pin by which we can predefine which function we want to perform. There are 4 output pin and another four output flags to signal for sign, carry out, overflow and zero output.

The functions that the ALU can compute are as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| OP code | Function no. | Operation | Description |
| 0 | F22 | B-A | 2’s complement subtraction |
| 1 | F13 | A-1 | Decrement |
| 2 | F2 | A AND B | Logical AND |
| 3 | F15 | B-1 | Decrement |
| 4 | F17 | -B | 2’s complement negation |
| 5 | F23 | 1111 | ALU Set |
| 6 | F3 | A OR B | Logical OR |
| 7 | F1 | 0000 | ALU Reset |
| 8 | F9 | A XNOR B | Logical Exclusive NOR |
| 9 | F6 | NOT B | Logical Complement |
| 10 | F21 | B-A-1 | 2’s complement subtraction with decrement |
| 11 | F18 | A+B+1 | 2’s complement addition with increment |
| 12 | F14 | B+1 | Increment |
| 13 | F16 | -A | 2’s complement negation |
| 14 | F11 | A-B | 2’s complement subtraction |
| 15 | F19 | A-B-1 | 2’s complement subtraction with decrement |

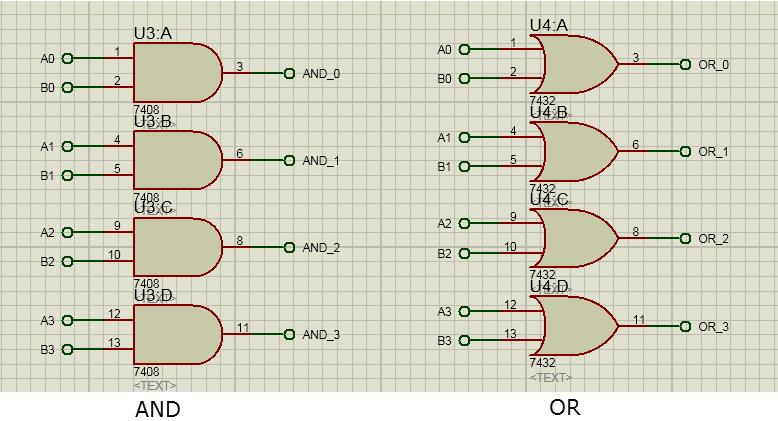
**Software Platform and IC’s:**

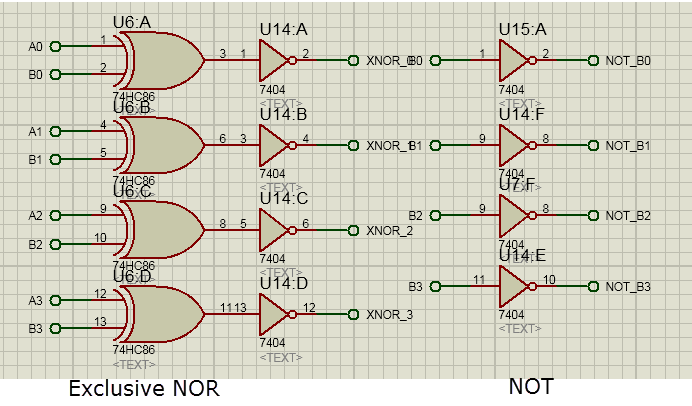
The 16 functions were designed and simulated in Proteus Software. For hardware visualization a Verilog code was written in Quartus software which will be uploaded in FPGA programming board.

**Functions descriptions:**

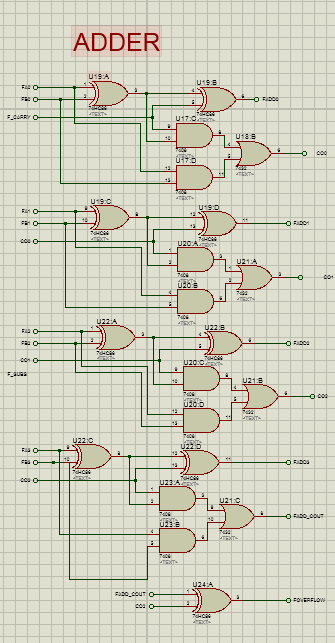
To developing the Arithmetic logic unit 74 series ICs were used.

* This is the logical operation circuit

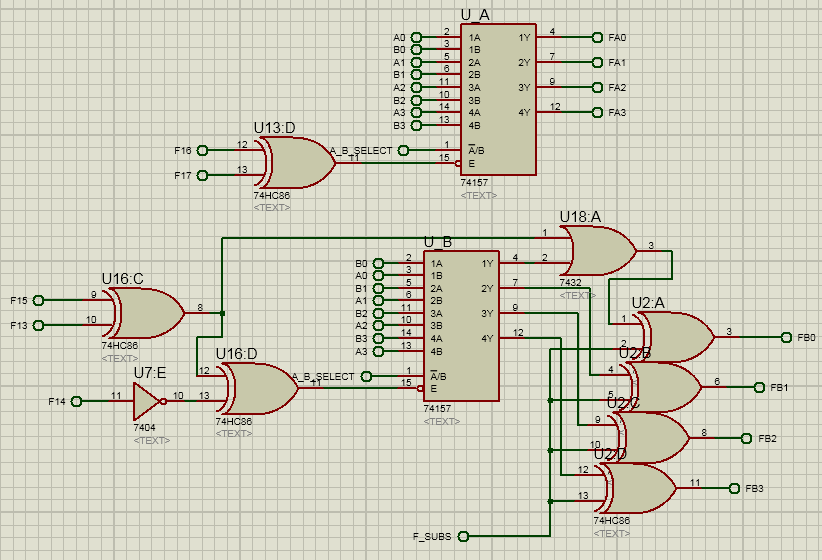


****

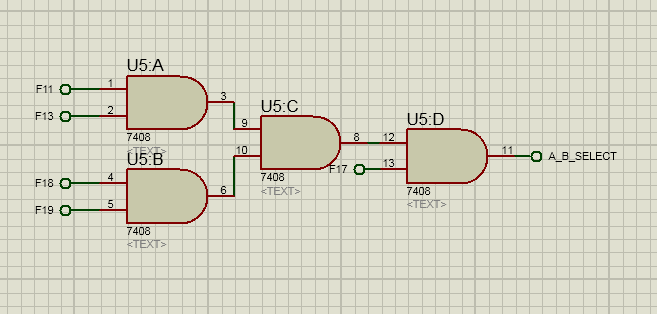
* This is the circuit for 4-bit ripple carry adder.

****

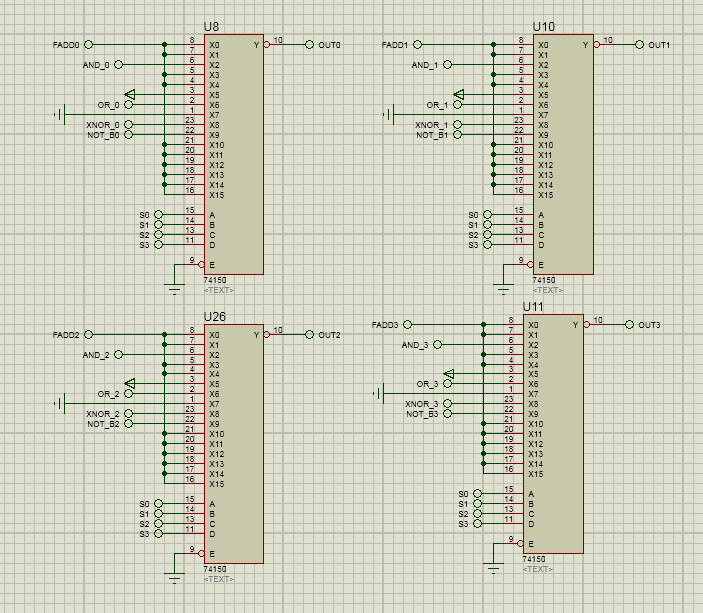
* This circuit detects whether A or B will be pass through A or B selection mux.



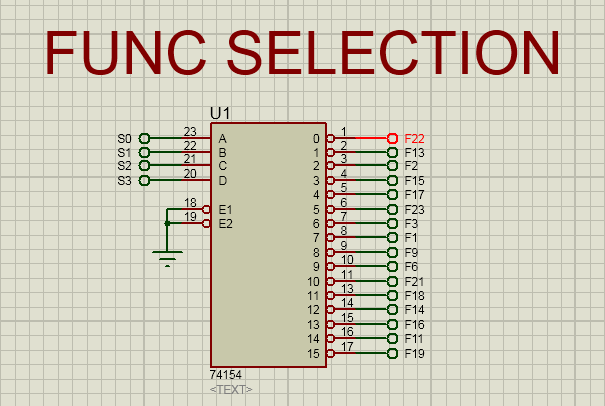
* Here A\_B\_Select pin will decide whether A or B bill be pass through mux.



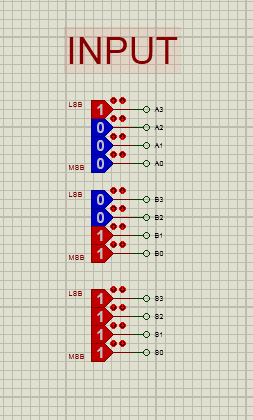
* This is the multiplexer circuit. 4 output bit pass through these 4 miltiplexers.

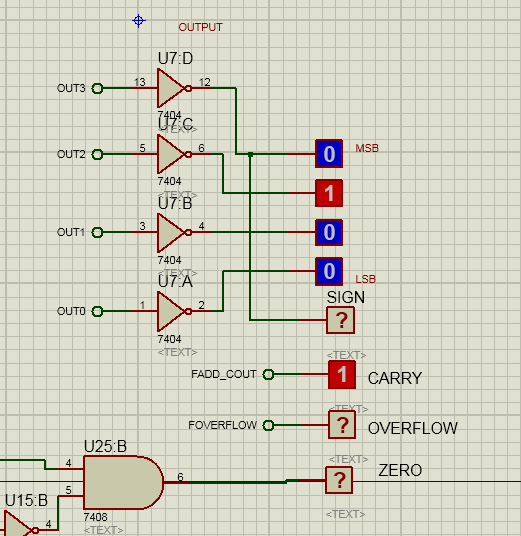


* As there are 16 functions and 4 selection bit. When any function are selected in selection bit, corresponding function execution circuit are passed through the below circuits.



* This is the input and output section of the Arithmetic logic unit.





**Verilog code:**

What we have done in the Proteus schematic, the same version of the arithmetic logic unit was developed in Verilog code so that we can simulate in the FPGA programming board. Few snippets of the code section are given below.

* This is the main module of the Verilog code. We have made 16 separate module for the 16 functions.

